

WHAT IS CLAIMED IS:

1 1. A method comprising:
2 generating event signals;
3 storing the event signals in a holding circuit;
4 producing response signals in a device under test (DUT)
5 in response to the event signals; and
6 evaluating the DUT based on the response signals from the
7 DUT and stored event signals received from the holding circuit
and.

1 2. The method of claim 1 comprising:
2 generating trigger signals; and
3 synchronizing each trigger signal with an event signal
such that the trigger signal occurs between a rising edge of
the event signal and a falling edge of the event signal.

1 3. The method of claim 1 comprising:
2 continuing to store an initial state of each event signal
3 in the holding circuit after transition of the event signal to
4 a subsequent state.

1 4. The method of claim 3 comprising:
2 applying a reset signal to the holding circuit.

1 5. The method of claim 1 wherein a minimum width of the
2 event-signal is 25 nano-seconds.

1 6. The method of claim 2 wherein a rising-edge of the event-
2 signal is in the range of 45 pico-seconds to 200 pico-seconds.

1 7. An apparatus comprising:

2 a driving circuit including an input and an output;
3 a first conductor including a first end and a second end;
4 a first input port for receiving a trigger signal coupled
5 to the input of the driving circuit;

6 a second input port for receiving an event signal coupled
7 to the first end of the first conductor;

8 an output port for outputting a hold signal coupled to
9 the second end of the first conductor; and

10 a second conductor, having an impedance higher than an
11 impedance of the first conductor, and coupled between the
12 output of the driving circuit and a connection point on the
13 first conductor.

1 8. The apparatus of claim 7 wherein the first conductor
2 includes a low impedance microstrip.

1 9. The apparatus of claim 7 wherein the second conductor
2 includes a high impedance microstrip having an impedance
3 higher than an impedance of the first conductor.

1 10. The apparatus of claim 7, wherein the driving circuit
2 comprises:

3 a third conductor, having a first end coupled to the
4 first input port for matching the impedance of the trigger
5 signal;

6 a matching circuit coupled to a second end of the third
7 conductor for matching the level of the trigger signal to the
8 driving circuit;

9 a sequential logic circuit, having an input coupled to an
10 output of the matching circuit, for holding a signal
11 corresponding to the state of the trigger signal; and

12 a buffer circuit having an enable input coupled to an
13 output of the sequential logic circuit and having an output
14 coupled to the output of the driving circuit.

11. The apparatus of claim 10 wherein the third conductor
includes a low impedance microstrip.

12. The apparatus of claim 10 wherein the sequential logic
circuit comprises a flip-flop.

13. The apparatus of claim 10 wherein the buffer circuit
comprises a tri-state-buffer.

14. The apparatus of claim 10 wherein the matching circuit
comprises a voltage divider.

15. The apparatus of claim 10 comprising a reset switch
circuit coupled to a reset input of the sequential logic

3 circuit for resetting the output of the sequential logic
4 circuit.

1 16. A system comprising:

2 a signal source for generating event signals and trigger
3 signals;

4 a holding circuit for receiving the event signals and
5 trigger signals, and for capturing the event signals;

6 a device under test (DUT) for producing response signals
7 in response to the event signals; and

8 a measuring device for evaluating the DUT based on the
9 response signals from the DUT and captured event signals from
10 the holding circuit.

11 17. The system of claim 16 wherein each trigger signal is
12 synchronized with an event signal such that the trigger signal
13 occurs between a rising edge of the event signal and a falling
14 edge of the event signal.

15 18. The system of claim 16 wherein the initial state of each
16 event signal is stored in the holding circuit after transition
17 of the event signal to a subsequent state.

18 19. The system of claim 16 wherein the holding circuit
19 comprises:

20 a driving circuit including an input and an output;

4 a first conductor including a first send and a second
5 end;
6 a first input port for receiving a trigger signal coupled
7 to the input of the driving circuit;
8 a second input port for receiving an event signal coupled
9 to the first end of the first conductor;
10 an output port for outputting a hold signal coupled to
11 the second end of the first conductor; and
12 a second conductor, having an impedance higher than an
13 impedance of the first conductor, and coupled between the
14 output of the driving circuit and a connection point on the
15 first conductor.

20. The system of claim 19 wherein the first conductor
includes a low impedance microstrip.

21. The system of claim 19 wherein the second conductor
includes a high impedance microstrip having an impedance
greater than an impedance of the first conductor.

22. The system of claim 19, the driving circuit comprising:
2 a third conductor, having a first end coupled to the
3 first input port for matching the impedance of the trigger
4 signal;

5 a matching circuit coupled to a second end of the third
6 conductor for matching the level of the trigger signal to the
7 driving circuit;

8 a sequential logic circuit, having an input coupled to an
9 output of the matching circuit, for holding a signal
10 corresponding to the state of the trigger signal; and

11 a buffer circuit having an enable input coupled to an
12 output of the sequential logic circuit and having an output
13 coupled to the output of the driving circuit.

23. The system of claim 21 wherein the third conductor
includes a low impedance microstrip.

24. The system of claim 21 wherein the sequential logic
circuit comprises a flip-flop.

25. The system of claim 21 wherein the buffer circuit
comprises a tri-state-buffer.

26. The system of claim 21 wherein the matching circuit
comprises a voltage divider.

27. The system of claim 21 comprising a reset switch circuit
coupled to a reset input of the sequential logic circuit for
resetting the output of the sequential logic circuit.